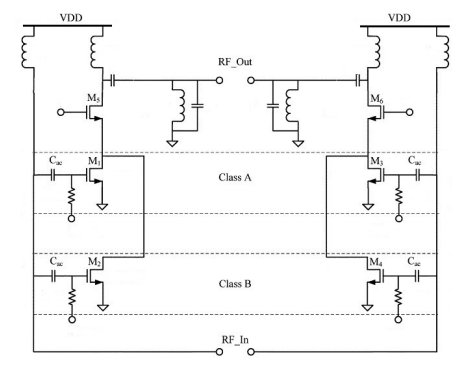
**Abstract:**  
Power amplifiers (PAs) are among the most crucial functional blocks in the radio frequency (RF) frontend for reliable wireless communication. PAs amplify and boost the input signal to the required output power. The signal is amplified to make it sufficiently high for the transmitter to propagate the required distance to the receiver. Attempted advancements of PA have focused on attaining high-performance RF signals for transmitters. Such PAs are expected to require low power consumption while producing a relatively high output power with a high efficiency. However, current PA designs in nanometer and micrometer complementary metal–oxide semiconductor (CMOS) technology present inevitable drawbacks, such as oxide breakdown and hot electron effect. A well-defined architecture, including a linear and simple functional block synthesis, is critical in designing CMOS PA for various applications.

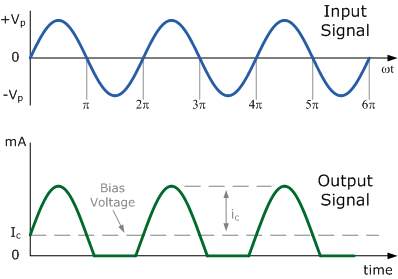
**Refarence Circuit Details :**

In the PA design in CMOS technology, two main issues must be addressed Oxide breakdown and the hot carrier effect. In this design, two amplifiers operate in parallel to improve the dynamic range and power efficiency. The input transistor M1 was biased with a fixed voltage of 1.2 V. The cascode configuration was formed by the CS transistors M1, M2, M3, and M4, and the CG transistors M5 and M6. The CS transistors form the transconductance of the class-A and the class-B PAs in order to provide more linear transconductance, which led to high power gain of 12dB. At low input levels, the class-A amplifier contributed the majority of the gain, and the class B amplifier had a very low gain. As the input level increased, the gain of the class- B amplifier increased, and its contribution to the overall gain increased proportionately. The outputs from both amplifiers were combined in the current domain with a slight overhead, thereby producing an improved isolation property and highpower efficiency of 44%. AC coupling capacitors and the matching network were used for the output impedance matching.{ \displaystyle \beta \_{\mathrm {Darlington} }\approx \beta \_{1}\cdot \beta \_{2}}

**Reference Circuit Diagram :**



Refarence Waveforms and Area Estimate:



**Refarence papers /Journals:**

Design Architectures of the CMOS Power Amplifier for 2.4 GHz ISM Band Applications:

1.Electrical and Electronics Engineering, Xiamen University Malaysia, Bandar Sunsuria, Sepang 43900, Selangor, Malaysia.

2. Electronic and Telecommunication Engineering, RMIT University, Melbourne, VIC 3000, Australia.

3. Electrical, Electronic and Systems Engineering, Universiti Kebangsaan Malaysia, Bangi 43600, Selangor, Malaysia.